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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/708,722	11/09/2000	Stephan J. Jourdan	2207/9800	2194

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WASHINGTON, DC 20005

EXAMINER
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O BRIEN, BARRY J

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 05/20/2004

10

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/708,722

Applicant(s)

JOURDAN ET AL.

Examiner

Barry J. O'Brien

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 November 2003 and 24 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 4.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. Claims 1-19 have been examined.

#### ***Papers Submitted***

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 11/26/03, Extension of Time as received on 2/24/04, Amendment A as received on 2/24/04, Correction of Inventorship as received on 2/24/04 and Corrected Formal Drawings as received on 2/24/04.

#### ***Correction of Inventorship***

3. In view of the papers filed on 2/24/04, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship, and accordingly, this application has been corrected in compliance with 37 CFR 1.48(a). The inventorship of this application has been changed by adding Lihu Rappoport as a named inventor.

The application will be forwarded to the Office of Initial Patent Examination (OIPE) for issuance of a corrected filing receipt, and correction of the file jacket and PTO PALM data to reflect the inventorship as corrected.

#### ***Specification***

Art Unit: 2183

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

#### ***Claim Objections***

6. Claims 16-18 are objected to because of the following informalities:

a. Claim 16 recites the limitation, "The method of claim 15" on its first line.

However, claim 15, as well as parent claim 14, is directed towards "A processing engine". Please correct the claim language to read, "The processing engine of claim 15". See also similar problems in claims 17 and 18 that require the same correction.

Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 5-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Art Unit: 2183

9. Claim 7 recites the limitation "the front-end system of claim 6" on its first line. There is insufficient antecedent basis for this limitation in the claim. While claim 5 recites the limitation, "a segment cache for a front-end system", it is claiming the segment cache, not the front-end system.

10. Claim 5 recites the limitation, "a plurality of cache entries to store instruction segments in reverse program order". It is unclear whether the instruction segments are being stored in reverse order, or the instructions that comprise the instruction segments are being stored in reverse order, as there is no real program order to the segments themselves. Please correct the claim language to more clearly define the metes and bounds of the invention. See also similar problems in claims 8 and 14 that require the same corrections. Because claims 6-7, 9-13 and 15-19 incorporate the limitations of claims 5, 8 and 14, respectively, claims 6-7, 9-13 and 15-19 are also rejected for the same reasons as claims 5, 8 and 14 listed above.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 1, 3-8, 12-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al., *Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing*, in further view of Johnson, U.S. Patent No. 5,924,092.

Art Unit: 2183

13. Regarding claim 1, Patel has taught an instruction segment comprising a plurality of instructions stored in sequential positions of a cache line (see Col.1 line 26 – Col.2 line 15). Patel has not explicitly taught storing the plurality of instructions in sequential positions of a cache line in reverse program order.

14. However, Johnson has taught the storing of blocks of data in reverse order so that those blocks that were in the first block of a data structure that are frequently accessed and modified will require less moving and fewer modifications after being placed at the last location of data structure, the fewer modifications resulting in improved performance (see Johnson, Col.4 lines 13-24). Because the traces of Patel are indexed, as well as accessed and modified, via their head (first) instructions (see Patel, Col.4 lines 23-31 and Col.5 lines 12-18), one of ordinary skill in the art would have found it obvious to modify the instruction segment of Patel to store the instructions of the instruction trace in reverse order so that the frequently accessed and modified head of the trace will be moved and modified fewer times so that performance is improved.

15. Regarding claim 3, Patel in view of Johnson has taught the instruction segment of claim 1, wherein the instruction segment is a trace (see Patel, Col.3 lines 2-12).

16. Regarding claim 4, Patel in view of Johnson has taught the instruction segment of claim 1, wherein the instruction segment is a basic block (see Patel, Col.2 lines 2-5).

17. Regarding claim 5, Patel has taught a segment cache (see “trace cache” of Fig.1) for a front-end system in a processor, comprising a plurality of cache entries to store instruction segments (see Col.1 line 26 – Col.2 line 15). Patel has not explicitly taught storing the instruction segments in reverse program order.

Art Unit: 2183

18. However, Johnson has taught the storing of blocks of data in reverse order so that those blocks that were in the first block of a data structure that are frequently accessed and modified will require less moving and fewer modifications after being placed at the last location of data structure, the fewer modifications resulting in improved performance (see Johnson, Col.4 lines 13-24). Because the traces of Patel are indexed, as well as accessed and modified, via their head (first) instructions (see Patel, Col.4 lines 23-31 and Col.5 lines 12-18), one of ordinary skill in the art would have found it obvious to modify the instruction segment of Patel to store the instructions of the instruction trace in reverse order so that the frequently accessed and modified head of the trace will be moved and modified fewer times so that performance is improved.

19. Regarding claim 6, Patel in view of Johnson has taught an apparatus comprising:

- a. An instruction cache system (see Patel, “instruction cache” of Fig.1),
- b. An instruction segment system, comprising:
  - I. A fill unit (see Patel, “fill unit” of Fig.1) provided in communication with the instruction cache system, the segment cache of claim 5 included therein (see Patel, Fig.1),
- c. A selector (see Patel, “selection logic” of Fig.1) coupled to an output of the instruction cache system and to an output of the segment cache (see Patel, Fig.1).

20. Regarding claim 7, Patel in view of Johnson has taught the front-end system of claim 6, wherein the instruction segment system further comprises a segment predictor (see Patel, “multiple branch predictor” of Fig.1) provided in communication with the segment cache. Here, when the multiple branch predictor is coupled with the trace cache and mediated by the selection

Art Unit: 2183

logic, it effectively predicts segments because the basic blocks stored in the trace cache all begin with branches (see Patel, Col.5 lines 5-29).

21. Regarding claim 8, Patel has taught a method for storing instruction segments in a processor, comprising:

- a. Building an instruction segment based on program flow (see Col.1 line 26 – Col.2 line 15),
- b. Storing the instruction segment in a cache (see Col.1 line 26 – Col.2 line 15).

22. Patel has not explicitly taught wherein the instruction segment is stored in reverse program order.

23. However, Johnson has taught the storing of blocks of data in reverse order so that those blocks that were in the first block of a data structure that are frequently accessed and modified will require less moving and fewer modifications after being placed at the last location of data structure, the fewer modifications resulting in improved performance (see Johnson, Col.4 lines 13-24). Because the traces of Patel are indexed, as well as accessed and modified, via their head (first) instructions (see Patel, Col.4 lines 23-31 and Col.5 lines 12-18), one of ordinary skill in the art would have found it obvious to modify the instruction segment of Patel to store the instructions of the instruction trace in reverse order so that the frequently accessed and modified head of the trace will be moved and modified fewer times so that performance is improved.

24. Regarding claim 12, Patel in view of Johnson has taught the method of claim 8, wherein the instruction segment is a trace (see Patel, Col.3 lines 2-12).

25. Regarding claim 13, Patel in view of Johnson has taught the method of claim 8, wherein the instruction segment is a basic block (see Patel, Col.2 lines 2-5).



Art Unit: 2183

26. Regarding claim 14, Patel has taught a processing engine, comprising:

- a. A front-end stage to build and store instruction segments (see Col.1 line 26 – Col.2 line 15),
- b. An execution unit (see “HPS Execution Core” in Fig.1) in communication with the front end stage (see Col.5 line 30 – Col.6 line 4).

27. Patel has not explicitly taught building and storing the instruction segments in reverse program order.

28. However, Johnson has taught the storing of blocks of data in reverse order so that those blocks that were in the first block of a data structure that are frequently accessed and modified will require less moving and fewer modifications after being placed at the last location of data structure, the fewer modifications resulting in improved performance (see Johnson, Col.4 lines 13-24). Because the traces of Patel are indexed, as well as accessed and modified, via their head (first) instructions (see Patel, Col.4 lines 23-31 and Col.5 lines 12-18), one of ordinary skill in the art would have found it obvious to modify the instruction segment of Patel to store the instructions of the instruction trace in reverse order so that the frequently accessed and modified head of the trace will be moved and modified fewer times so that performance is improved.

29. Regarding claim 15, Patel in view of Johnson has taught the processing engine of claim 14, wherein the front-end stage comprises:

- a. An instruction cache system (see Patel, “instruction cache” of Fig.1),
- b. An instruction segment system, comprising:
  - I. A fill unit (see Patel, “fill unit” of Fig.1) provided in communication with the instruction cache system (see Patel, Fig.1),

Art Unit: 2183

II. A segment cache (see “trace cache” of Fig.1),

c. A selector (see Patel, “selection logic” of Fig.1) coupled to an output of the instruction cache system and to an output of the segment cache (see Patel, Fig.1).

30. Regarding claim 17, Patel in view of Johnson has taught the method of claim 15, wherein the instruction segments are traces (see Patel, Col.3 lines 2-12).

31. Regarding claim 18, Patel in view of Johnson has taught the method of claim 15, wherein the instruction segments are basic blocks (see Patel, Col.2 lines 2-5).

32. Regarding claim 19, Patel in view of Johnson has taught the method of claim 15, wherein the instruction segment cache system further comprises a segment predictor (see Patel, “multiple branch predictor of Fig.1) provided in communication with the segment cache. Here, when the multiple branch predictor is coupled with the trace cache and mediated by the selection logic, it effectively predicts segments because the basic blocks stored in the trace cache all begin with branches (see Patel, Col.5 lines 5-29).

33. Claims 2, 9-11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al., *Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing*, in view of Johnson, U.S. Patent No. 5,924,092, in further view of Peled et al., U.S. Patent No. 6,076,144.

34. Regarding claim 2, Patel in view of Johnson has taught the instruction segment of claim 1, but has not explicitly taught wherein the instruction segment is an extended block.

35. However, Peled has taught trace segments which have multiple entry points and a single exit that allow redundant code segments to be eliminated from the trace cache, thereby improving cache utilization (see Peled, Col.1 lines 60-63, Col.4 lines 13-37, and Fig.3). Because

Art Unit: 2183

the specification has defined an extended block to have multiple entry points and a single exit point (see p.2 of Specification), one of ordinary skill in the art would have found it obvious to modify the instruction segments of Patel to allow for multiple entry points and a single exit so that redundant code segments could be eliminated from the trace cache and performance could be improved.

36. Regarding claim 9, Patel in view of Johnson have taught the method of claim 9, but have not explicitly taught wherein the method further comprises:

- a. Building a second instruction segment based on program flow,
- b. If the first and second instruction segments overlap, extending the first instruction segment to include non-overlapping instructions from the second instruction segment.

37. However, Peled has taught building a second instruction segment based on program flow and subsequently extending the first instruction segment to include the non-overlapping instructions from the second instruction segment if the two segments overlap (see Col.4 lines 13-37) in order to reduce the degree of code redundancy in the trace cache (see Col.1 lines 60-63). One of ordinary skill in the art would have recognized that it is desirable to reduce redundancy within a trace cache so that the cache can be more effectively used and more different traces stored. Therefore, one of ordinary skill in the art would have found it obvious to extend an existing instruction segment to include non-overlapping instructions from a second instruction segment in order to reduce trace cache redundancy.

38. Regarding claim 10, Patel in view of Johnson in further view of Peled has taught the method of claim 9, but has not explicitly taught wherein the extending comprises storing the non-

Art Unit: 2183

overlapping instructions in the cache in reverse program order in successive cache positions adjacent to the instructions from the first instruction segment.

39. However, Patel in view of Johnson has taught that instructions in instruction segments are stored in reverse program order (see paragraphs 21-23 above). Because, an extended segment is still an instruction segment, one of ordinary skill in the art would have found it obvious to also store the extended instruction segments in reverse program order.

40. Regarding claim 11, Patel in view of Johnson has taught the method of claim 8, but has not explicitly taught wherein the instruction segment is an extended block.

41. However, Peled has taught trace segments which have multiple entry points and a single exit that allow redundant code segments to be eliminated from the trace cache, thereby improving cache utilization (see Peled, Col.1 lines 60-63, Col.4 lines 13-37, and Fig.3). Because the specification has defined an extended block to have multiple entry points and a single exit point (see p.2 of Specification), one of ordinary skill in the art would have found it obvious to modify the instruction segments of Patel to allow for multiple entry points and a single exit so that redundant code segments could be eliminated from the trace cache and performance could be improved.

42. Regarding claim 16, Patel in view of Johnson has taught the method of claim 15, but has not explicitly taught wherein the instruction segments are extended blocks.

43. However, Peled has taught trace segments which have multiple entry points and a single exit that allow redundant code segments to be eliminated from the trace cache, thereby improving cache utilization (see Peled, Col.1 lines 60-63, Col.4 lines 13-37, and Fig.3). Because the specification has defined an extended block to have multiple entry points and a single exit

Art Unit: 2183

point (see p.2 of Specification), one of ordinary skill in the art would have found it obvious to modify the instruction segments of Patel to allow for multiple entry points and a single exit so that redundant code segments could be eliminated from the trace cache and performance could be improved.

### ***Response to Arguments***

44. Applicant's arguments, see pages 5-8 of the present amendment filed 2/24/04, with respect to the rejection(s) of claim(s) 1-19 under 35 USC § 102 and 35 USC § 103, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in further view of Johnson, U.S. Patent No. 5,924,092, which has taught the storing of data blocks in reverse order (see above rejections).

### ***Conclusion***

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

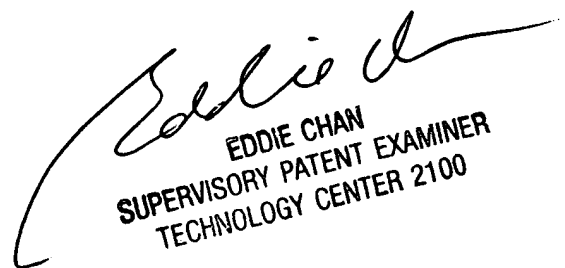
Art Unit: 2183

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

47. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien  
Examiner  
Art Unit 2183

BJO  
5/12/2004

  
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